

**IN THE DRAWINGS**

The Office Action states that corrected drawings for Figures 2, 3, and 5 in compliance with 37 CFR 1.121(d) are required in reply to the Office Action to avoid abandonment of the application.

Amended drawings are supplied herewith, each identified as “REPLACEMENT SHEET” of the drawings. Figures 2, 3, and 5 have the legend “Prior Art” added.

**REMARKS**

This responds to the Office Action dated May 19, 2005.

Claims 5 and 13 are amended; as a result, claims 1-10, 12-28, and 30-40 are now pending in this application.

**§102 Rejection of the Claims**

Claims 5-10 and 12-28 were rejected under 35 USC § 102(e) as being anticipated by Chehrazi et al. (U.S. 6,301,599, “Chehrazi”). Applicant respectfully traverses the rejection. To anticipate a claim the reference must teach every element of the claim.<sup>1</sup>

*Regarding 5-10, 12:*

Applicant cannot find in Chehrazi, among other things,  
a plurality of logic circuits coupled to ones of said plurality of transistors to output  
Booth encoded signals, wherein said Booth encoded signals are substantially gate  
delay-matched from the transistors to the output of said Booth encoder circuit,

as presently recited or incorporated in the claims. Instead, the circuit in Chehrazi varies from several gate delays to as few as one gate delay.<sup>2</sup> Additionally, Chehrazi refers to a critical path which encounters a delay approximately equivalent to four NAND gates,<sup>3</sup> and Chehrazi defines a critical path as the logical flow through a circuit which takes the longest time to complete.<sup>4</sup> Thus, Chehrazi refers to managing critical paths instead of matching signal delays.

*Regarding 13-21:*

Applicant cannot find in Chehrazi, among other things,  
comprising logic to receive a plurality of multiplier bits and complements of said  
multiplier bits, said logic to output Booth encoded signals based on said multiplier  
bits and complements of said multiplier bits, said logic configured to have a  
substantially matched delay of three gate delays from an input of said multiplier  
circuit to an output of said multiplier circuit,

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<sup>1</sup> M.P.E.P. § 2131.

<sup>2</sup> Chehrazi Fig. 4.

<sup>3</sup> Chehrazi, col. 6, lines 63-65, and Figs. 4 and 5.

<sup>4</sup> Chehrazi, col. 1, lines 65-67.

as presently recited or incorporated in the claims. Instead, the circuit in Chehrazi has as few as one gate delay.<sup>5</sup>

*Regarding claim 22-24:*

Applicant is unable to find in Chehrazi, among other things, logic including a plurality of transistors, a plurality of NAND gates and a plurality of inverters configured to output delay-matched Booth encoded signals based on said multiplier bits and said complements,

as recited or incorporated in the claims. The cited portions of Chehrazi refer to a critical path which encounters a delay approximately equivalent to four NAND gates,<sup>6</sup> and Chehrazi defines the critical path as the logical flow through a circuit which takes the longest time to complete.<sup>7</sup> Thus, Chehrazi refers to managing critical paths instead of matching signal delays. Additionally, the circuit in Chehrazi varies from several gate delays to as few as one gate delay.<sup>8</sup> Therefore, the cited portions of Chehrazi do not refer to output delay-matched Booth encoded signals.

*Regarding claims 25-28:*

Applicant cannot find in the cited portions of Chehrazi, among other things, wherein said Booth encoded signals are substantially delay-matched at an output of said Booth encoder circuit,

as recited or incorporated in the claims. The circuit referred to in Chehrazi varies from several gate delays to as few as one gate delay.<sup>9</sup>

Additionally, Applicant cannot find

a second subcircuit to receive at least one multiplier bit and complements of at least one multiplier bit, said second subcircuit to provide a signal to second logic circuits, said second logic circuits to output one Booth encoded signal; a third subcircuit to receive at least one multiplier bit and complements of at least one multiplier bit, said third subcircuit to provide a signal to third logic circuits, said third logic circuits to output one Booth encoded signal,

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<sup>5</sup> *Chehrazi*, Fig. 4.

<sup>6</sup> *Chehrazi*, col. 6, lines 63-65, and Figs. 4 and 5.

<sup>7</sup> *Chehrazi*, col. 1, lines 65-67.

<sup>8</sup> *Chehrazi*, Fig. 4.

<sup>9</sup> *Id.*

as recited or incorporated in the claims. The Office Action calls the circuit in Chehrazi that provides the S2 output the “second subcircuit,” and calls the circuit that provides S\_2 output the “third subcircuit”.<sup>10</sup> In Fig. 4 of Chehrazi, these circuits provide no other signals. Claim 25 recites the second and third subcircuits providing a signal to second and third logic circuits which each output a Booth encoded signal. Therefore, the circuit in Chehrazi does not have both second and third subcircuits *and* second and third logic circuits.

Applicant respectfully requests reconsideration and allowance of claims 5-10 and 12-28.

Claims 30-31 and 33-40 were rejected under 35 USC § 102(b) as being anticipated by Lee et al. (U.S. 5,818,743, “Lee”). Applicant respectfully traverses the rejection.

*Regarding claims 30-31, 33-36:*

Applicant cannot find in Lee, among other things,

A partial products generator circuit comprising a first multiplexing device having a plurality of first transistors to receive Booth encoded signals and to provide a first partial products output; and a second multiplexing device having a plurality of second transistors to receive said Booth encoded signals and multiplexed data from said first multiplexing device and to provide a second partial products output,

as recited or incorporated in the claims.

The Mux devices in Lee, that are referred to in the middle of page 9 of the Office Action, apparently receive inputs from Full Adders<sup>11</sup> rather than multiplexed data from another multiplexing device. Additionally, the multiplexing devices 244' and 244'' of Lee provide different partial products.<sup>12</sup> Therefore, the devices of Lee do not provide first and second partial products outputs of a partial products generator circuit.

*Regarding claims 37-40:*

Applicant cannot find in Chehrazi, among other things,

a partial products generator circuit comprising a multiplexing device to receive Booth encoded signals and to provide a first partial product output for a first bit of a multiplicand based at least on multiplexed data received from a previous multiplexing device,

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<sup>10</sup> Office Action, pg. 4.

<sup>11</sup> Lee, Fig. 9A and col. 6 lines 38-49.

<sup>12</sup> Lee, Figs. 1 and 7A and col. 6 lines 38-49.

as presently recited in the claims. The Mux devices in Lee, that are referred to in the middle of page 9 of the Office Action, apparently receive inputs from Full Adders<sup>13</sup> rather than receive multiplexed data from a previous multiplexing device. Additionally, the multiplexing devices 244' and 244" of Lee comprise different partial products circuits.<sup>14</sup>

Applicant respectfully requests reconsideration and allowance of claims 30-31 and 33-40.

**§103 Rejection of the Claims**

Claims 1-4 were rejected under 35 USC § 103(a) as being unpatentable over Chehrazi et al. (U.S. 6,301,599) in view of Lee et al. (U.S. 5,818,743). Applicant respectfully traverses the rejection.

In order to establish a *prima facie* case of obviousness the cited reference or references must teach or suggest all the claim limitations.<sup>15</sup>

Applicant is unable to find in the proposed combination of Chehrazi and Lee a teaching or suggestion of, among other things,

a partial products generating circuit having a first multiplexing device to receive said Booth encoded signals and to provide a first partial products output, and a second multiplexing device to receive said Booth encoded signals and multiplexed data from said first multiplexing device and to provide a second partial products output,

as recited or incorporated in the claims. The Mux devices in Lee (244' and 244"), that are referred to in the middle of page 9 of the Office Action, apparently receive inputs from Full Adders<sup>16</sup> instead of Booth encoded signals. Additionally, Lee does not teach or suggest a second multiplexing device to receive said Booth encoded signals and multiplexed data from said first multiplexing device and to provide a second partial products output. Further, devices 244' and 244" in Lee are apparently each used to create a separate partial product<sup>17</sup> and thus do not create first and second outputs of a partial product.

Applicant respectfully requests reconsideration and allowance of claims 1-4.

<sup>13</sup> Lee, Fig. 9A and col. 6 lines 38-49.

<sup>14</sup> Lee, Figs. 1 and 7A and col. 6 lines 38-49.

<sup>15</sup> M.P.E.P. 2143.03.

<sup>16</sup> Lee, Fig. 9A and col. 6 lines 38-49.

<sup>17</sup> Lee, Figs. 1, 7A, and col. 4 lines 8-17.

**AMENDMENT UNDER 37 C.F.R. 1.116 – EXPEDITED PROCEDURE**

Serial Number: 10/073,190

Filing Date: February 13, 2002

Title: BOOTH ENCODER AND PARTIAL PRODUCTS CIRCUIT

Assignee: Intel Corporation

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Dkt: 884.A25US1 (INTEL)

Claim 32 was rejected under 35 USC § 103(a) as being obvious over Lee et al. (U.S. 5,818,743). Applicant respectfully traverses the rejection.

Claim 32 depends on base claim 30 and is construed to incorporate all the elements of the base claim. Applicant believes that claim 32 is allowable at least for the reason that Lee fails to teach or suggest all elements of claim 30 incorporated into claim 32. Applicant respectfully requests reconsideration and allowance of claim 32.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9592 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KENNETH Y. NG

By his Representatives,

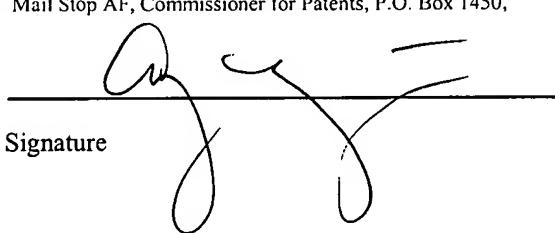
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**CERTIFICATE UNDER 37 CFR 1.8:** The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 21<sup>st</sup> day of November, 2005.